**BAHRIA UNIVERSITY (KARACHI CAMPUS**)

**Computer Architecture & Logic Design (CEN- 220)**

**Assignment 02**

**Fall 2023**

**Class: BSE 3B Shift: Morning**

**Course Instructor: Engr. Ramsha Mashood Due Date: 06 Nov 2023**

**Assignment Date: 26 Oct 2023 Marks: 05 Points**

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Question:

Imagine you are working as a computer architect for a startup company developing innovative wearable devices. Your team is designing a new wearable device that focuses on real-time health monitoring, fitness tracking, and providing personalized health recommendations. The device is expected to handle various sensor inputs, process complex algorithms for health analysis, and communicate the results to the user in real-time. Your task is to design the computer architecture for this wearable device.

Considering the wearable device scenario described, apply the principles taught in computer architecture and organization. Discuss the key aspects of the architecture you would design, including the processor, memory hierarchy, I/O interfaces, and any specific techniques you would employ to optimize the system's performance and power efficiency. Explain your choices based on Lectures. Provide sufficient Justification for the given Scenario based on authentic Source.

Answer:

The design of a wearable device that focuses on real-time health monitoring, fitness tracking, and providing personalized health recommendations requires a computer architecture that is optimized for performance and power efficiency. The key aspects of the architecture that would be designed include the processor, memory hierarchy, and I/O interfaces.

1. Processor:

The processor is the heart of the wearable device, and it must be powerful enough to handle various sensor inputs and process complex algorithms for health analysis. A low-power processor such as the ARM Cortex-M4 or M7 would be ideal for this scenario. These processors are designed to consume minimal power while providing high performance.

1. Memory Hierarchy:

The memory hierarchy is an essential component of the computer architecture that would design. The wearable device must have a memory hierarchy that is optimized for performance and power efficiency. The memory hierarchy should include a small amount of fast memory such as SRAM or cache memory to store frequently accessed data and instructions. The main memory should be DRAM or SDRAM to provide a larger storage capacity. The secondary storage should be Flash Memory to provide non-volatile storage.

1. I/O Interfaces:

The I/O interfaces are the channels through which the wearable device communicates with the outside world. The I/O interfaces should be designed to minimize power consumption while providing high-speed data transfer. The I/O interfaces should include Bluetooth Low Energy (BLE), Wi-Fi, and NFC. These interfaces are designed to consume minimal power while providing high-speed data transfer.

1. Optimization Techniques:

To optimize the system's performance and power efficiency, the following techniques can be employed:

-**Power Management:** The wearable device should have a power management system that is designed to minimize power consumption. The power management system should include features such as power gating, dynamic voltage scaling, and clock gating.

**-Data Compression:** The data generated by the sensors can be compressed to reduce the amount of data that needs to be processed. This technique can reduce the power consumption of the processor and memory.

**-Algorithm Optimization:** The algorithms used for health analysis should be optimized to minimize the number of computations required. This technique can reduce the power consumption of the processor.

Conclusion:

In conclusion, the design of a wearable device that focuses on real-time health monitoring, fitness tracking, and providing personalized health recommendations requires a computer architecture that is optimized for performance and power efficiency. The key aspects of the architecture that would be designed include the processor, memory hierarchy, and I/O interfaces. The optimization techniques that can be employed include power management, data compression, and algorithm optimization.

Source:

<https://en.wikipedia.org/wiki/Wearable_computer>

<https://teksun.com/blog/how-to-design-successful-wearable-iot-devices/>.

<https://www.techinsights.com/technology-guides/guide-processors-iot-wearables>.

<https://www.tutorialspoint.com/discuss-the-i-o-interface-in-computer-architecture>.

<https://www.elprocus.com/memory-hierarchy-in-computer-architecture/>.

<https://www.studytonight.com/computer-architecture/memory-organization>.